IN THE CLAIMS:

1. (Previously Presented) A method of manufacturing a laterally diffused metal oxide semiconductor (LDMOS) device, comprising:

forming first and second isolation structures within a substrate;

forming a lightly-doped source/drain region between the first and second isolation structures with only a first dopant and without the use of a mask; and

creating a gate over the lightly-doped source/drain region.

2. (Original) The method as recited in Claim 1 wherein forming includes forming a lightly-doped source/drain region with a first N-type dopant.

3. (Original) The method as recited in Claim 2 wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm^2 to about 1E13 atoms/cm^2.

Claim 4 (Canceled)

5. (Original) The method as recited in Claim 1 further including diffusing a second dopant at least partially across the lightly-doped source/drain region and under the gate to form a first portion of a channel.

6. (Previously Presented) The method as recited in Claim 5 wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose ranging from about

1E13 atoms/cm^2 to about 1E14 atoms/cm^2.

7. (Previously Presented) The method as recited in Claim 5 wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose about 100 times higher than an implant dose of the first dopant.

8. (Original) The method as recited in Claim 5 further including placing a heavy concentration of the first dopant in a region adjacent a source side of the gate, and in the lightly-doped source/drain region adjacent a drain side of the gate.

9. (Original) The method as recited in Claim 8 wherein placing includes placing the heavy concentration of the first dopant in the lightly-doped source/drain region a distance ranging from about 2000 nm to about 3000 nm from the drain side of the gate.

Claim 10 (Canceled)

11. (Withdrawn) A method of manufacturing an integrated circuit, comprising:

fabricating laterally diffused metal oxide semiconductor (LDMOS) transistors, including:

forming first and second isolation structures in a substrate;

forming a lightly-doped source/drain region between the first and second isolations structures and with only a first dopant; and

creating a gate over the lightly-doped source/drain region;

depositing interlevel dielectric layers over the LDMOS transistors; and

creating interconnect structures in the interlevel dielectric layers and interconnecting the LDMOS transistors to form an operative-integrated circuit.

12. (Withdrawn) The method as recited in Claim 11 wherein forming includes forming a lightly-doped source/drain region with a first N-type dopant.

13. (Withdrawn) The method as recited in Claim 12 wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm^2 to about 1E13 atoms/cm^2.

Claim 14 (Canceled)

15. (Withdrawn) The method as recited in Claim 11 further including diffusing a second dopant at least partially across the lightly-doped source/drain region and under the gate to form a first portion of a channel.

16. (Withdrawn) The method as recited in Claim 15 wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose ranging from about 1E13 atoms/cm^2 to about 1E14 atoms/cm^2.

17. (Withdrawn) The method as recited in Claim 15 wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose about 100 times higher than an

implant dose of the first dopant.

18. (Withdrawn) The method as recited in Claim 15 further including placing a heavy concentration of the first dopant in a region adjacent a source side of the gate, and in the lightly-doped source/drain region adjacent a drain side of the gate.

Claim 19 (Canceled)

20. (Withdrawn) The method as recited in Claim 18 wherein placing includes placing an implant dose of the first dopant ranging from about 1E15 atoms/cm^2 to about 1E16 atoms/cm^2.

21. (Previously Presented) The method as recited in Claim 1 wherein forming the lightly-doped source/drain region includes forming the lightly-doped source/drain region using a blanket implant process over the entire substrate.

22. (Withdrawn) The method as recited in Claim 11 wherein forming the lightly-doped source/drain region includes forming the lightly-doped source/drain region using a blanket implant process over the entire substrate.

23. (Withdrawn) A method of manufacturing a laterally diffused metal oxide semiconductor (LDMOS) device, comprising:

forming first and second isolation structures within a substrate, the first isolation structure

having a first edge and a second edge and the second isolation structure having a third edge and a fourth edge;

forming a lightly-doped source/drain region between the first and second isolation structures with only a first dopant, the lightly-doped source/drain region in contact with the second edge of the first isolation structure and the third edge of the second isolation structure; and

creating a gate over the lightly-doped source/drain region and between the first and second isolation structures.

24. (Withdrawn) The method as recited in Claim 23 wherein the first and second isolation structures are first and second field oxide isolation structures.